# GP-IP Clock Generator Module

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This note describes an IndustryPack-base clock generator module. Output from the generator conforms to the Fermilab TCLK protocol that carries eight-bit events encoded on a 10 MHz signal. Events may be placed on the clock from external pulse inputs, from events detected on an incoming clock, and from data written to the generator by the host computer. The generator includes provision for backup in case the incoming clock disappears.

Physically, the IndustryPack Module is a 1.8" by 3.9" circuit board that contains two high density 50-pin "D" female connectors as defined by the GreenSpring IndustryPack specification. This specification is a public domain definition of a small mezzanine board for use in microprocessor-based systems.

The clock generator uses the General Purpose IP module, (GP-IP). Figure 1 is a diagram of the GP-IP module showing the parts placement including the two 50-pin connectors, one logic interface and one for user I/O signals. This is a commercially available general purpose programmable module that contains an Altera 10K40 FPGA, two tapped delay lines, 256kBytes of static RAM, a 10 MHz crystal oscillator, two clock receiver discriminators, and an 8-pin PROM socket used to hold a 1Mbit serial PROM that programs the Alters chip after power-up. An 8-bit option switch is available to select various operating options. Implementing various circuit designs using this module only requires plugging in the serial PROM containing the design information needed to configure the Altera gate array.

I/O for the clock generator board includes a TClk input, an input for 10 MHz signal for backup, an input for 15 Hz backup, 16 pulsed event input trigger signals, and outputs for the encoded clock, status bits to indicate when the 15 Hz and the 10 MHz from the input clock are no longer present. Several test point signals are also available on the IP module's user connector.

The Altera chip contains the following circuitry:

- IP interface logic
- TClk decoder
- Sixteen event input latches
- Prioritizer for the 16 input latches
- Prioritizer for input-triggered events, decoded events and computer generated events
- Serializer and Manchester encoder

A block diagram of the clock generator is given in Figure 2. In normal operation the clock generator, used with the Tevatron clock, decodes the incoming clock and passes all the events as they are detected on the incoming clock. Pulse input events are latched individually, prioritized, and output as $Xx events, where X is the 4-bit value set into the IP module's option DIP switch. A separate 8-bit latch can be written by the IP's host computer to address Base+1. A *write* to this location causes the latched value to be encoded as an event on the serial clock output. Sources of events are prioritized as trigger input events, decoded events, and computer events, in that order. A 4-word FIFO is included in the design to allow a close packed group of decoded events to be output without interference from pulsed events that are higher in priority. The computer events are given the lowest priority because they would typically be settings to the local station that arrived as a network message and have less precise timing than a pulse input trigger or a decoded event.

This module functions as dedicated hardware. When power is applied, the Altera gate array is programmed from the EPC1 serial PROM, and the module is immediately ready to operate. The only host computer interaction is the writing of computer events to be encoded onto the outgoing clock signal. These 8-bit values are written as a byte to the IP module BaseAddress+1. A word write to the IP module's BaseAddress is also allowed. The event value is placed in the least significant byte of the word.

Pulsed events are encoded as a block of sixteen contiguous values. The value of the upper four bits of the encoded event are determined by the setting of bits 7..4 of an 8-bit surface mount switch included on the GP-IP module. The lower four bits of the encoded event depend on which input line was pulsed. Switch bit 3 determines whether incoming events that have a value within the range of pulsed event values, are blocked or passed through and encoded onto the output clock.

At Fermilab, the Tevatron clock, TClk, contains 60Hz, 720Hz and 1440 Hz events. These events may be blocked individually by setting option switches 0..2, respectively.

If this module is used where no TClk input is available, an external 10MHz signal may be used as the timebase. If no signal is detected on the TClk/Ext input, the module automatically switches to the onboard 10 MHz crystal oscillator. Similarly, if no 10/15 Hz event is detected, the module will look for an external pulse train to generate the 15Hz event. A 60 Hz or 120Hz pulse train may be used. The 15Hz output pulse train generated by the module may be used as one of the 16 pulsed inputs to encode the 15Hz event onto the output clock

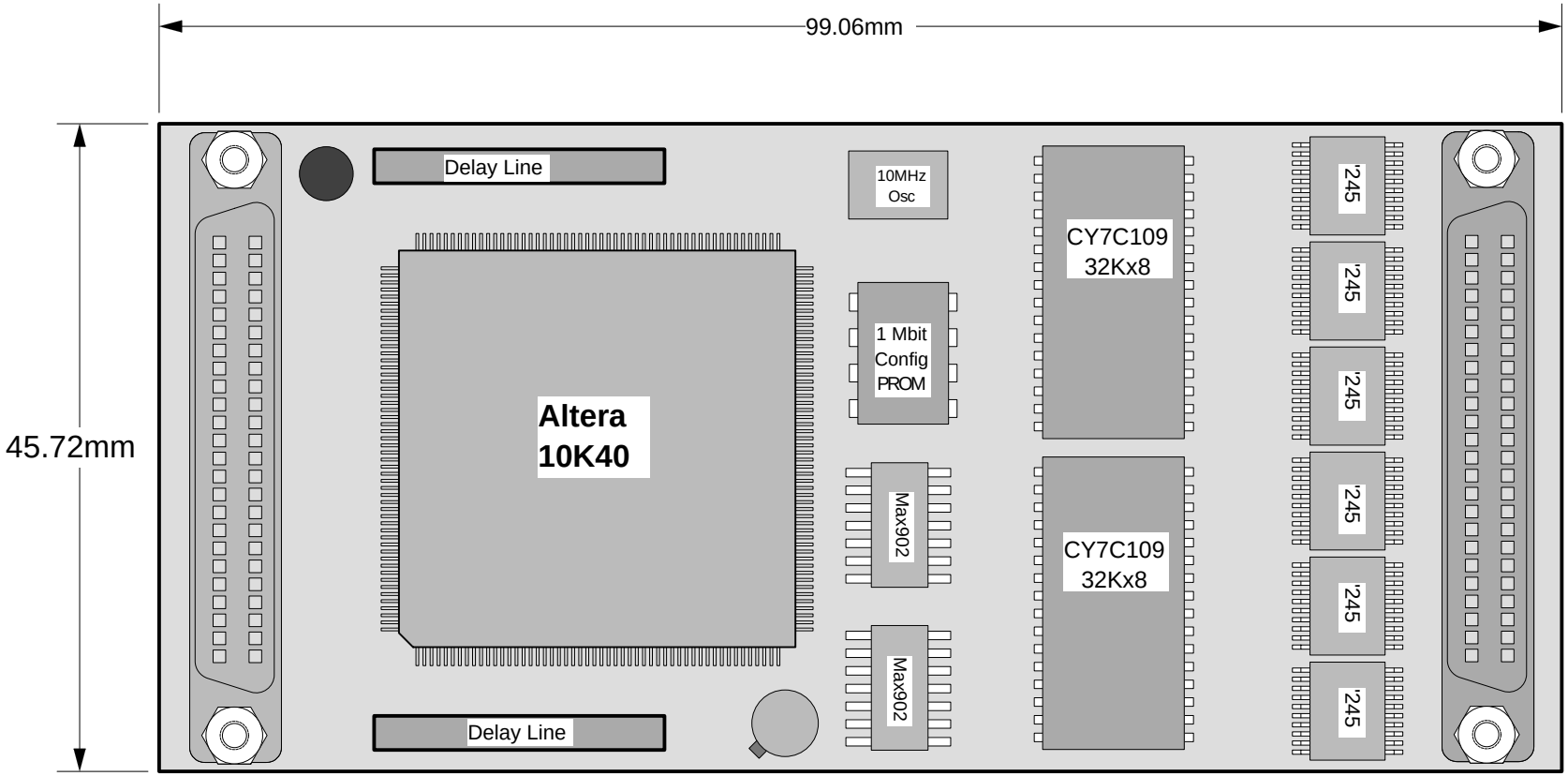


**Figure 1. Plan View of the GP-IP**

| | | |
|---|---|---|
| TITLE: *General Purpose IP* | | SIZE: **A** |
| PART NUMBER: *GPIP* | DRAWN BY: *M. Shea* | DATE: *2/10/98* |

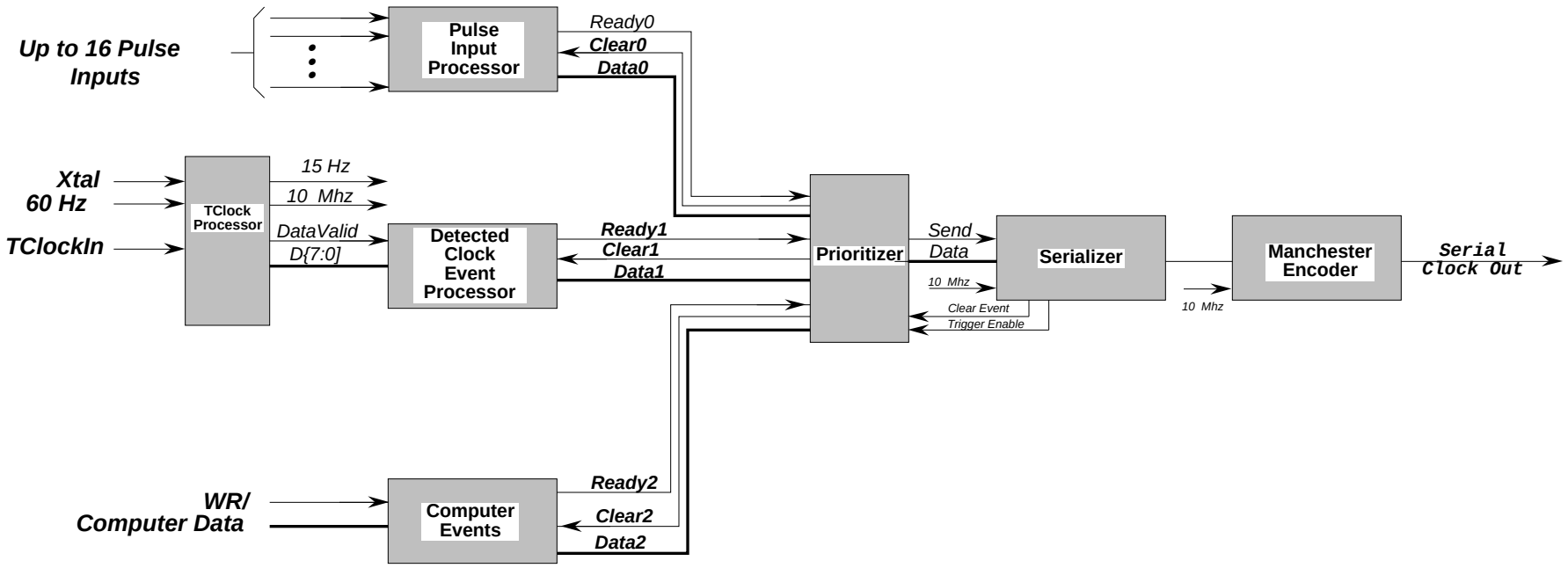


**Figure 2. GP-IP Based Clock Generator Block Diagram**

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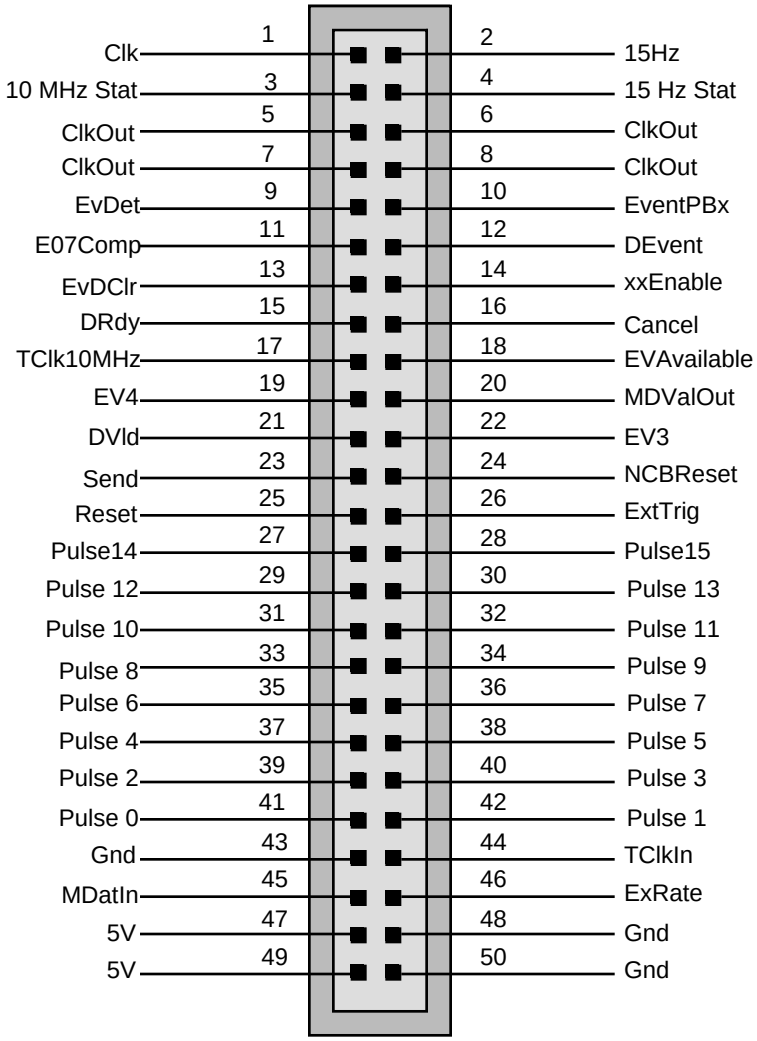


*Pin numbers of the IP module connector P2 are the same as for Carrier Board connector*

**Figure 3. GP-IP Clk Generator Pinout**